

## CLAIMS

Having thus described our invention in detail, what we claim as new and desire to secure by the Letters Patent is:

- 1 1. A semiconductor memory structure comprising:  
2  
3 at least one adjacent pair of trench storage memory cells present in a Si-containing  
4 substrate, each memory cell including a vertical transistor overlaying a trench capacitor;  
5  
6 strap outdiffusions present on each vertical sidewall of the trench storage memory cells,  
7 wherein said strap outdiffusions interconnect said vertical transistor and said trench  
8 capacitor of each memory cell to said Si-containing substrate; and  
9  
10 a punchthrough stop doping pocket located between each adjacent pair of trench storage  
11 memory cells, said punchthrough stop doping pocket is centered between said strap  
12 outdiffusions.
- 1 2. The semiconductor memory structure of Claim 1 wherein a plurality of adjacently  
2 paired trench storage memory cells are employed, and said punchthrough stop doping  
3 pockets are positioned at substantially the same location within the Si-containing  
4 substrate thereby eliminating alignment tolerance in the structure.
- 1 3. The semiconductor memory structure of Claim 1 wherein said trench capacitor  
2 comprises a buried plate diffusion region present about a storage trench, a node  
3 dielectric lining said storage trench and a N+ polysilicon layer present on said node  
4 dielectric.

- 1 4. The semiconductor memory structure of Claim 1 wherein said vertical transistor  
2 comprises a gate dielectric present on sidewalls of a storage trench and a N+ doped  
3 polysilicon gate conductor present on said gate dielectric.
- 1 5. The semiconductor memory structure of Claim 1 wherein said vertical transistor and  
2 said trench capacitor are separated by a trench top oxide layer.
- 1 6. The semiconductor memory structure of Claim 1 wherein said punchthrough doping  
2 pocket includes a P-type dopant.
- 1 7. The semiconductor memory structure of Claim 6 wherein said punchthrough doping  
2 pocket has a dopant concentration of about  $1E18\text{ cm}^{-3}$  or less.
- 1 8. The semiconductor memory structure of Claim 1 further comprising wordlines  
2 present atop each trench storage memory cell.
- 1 9. The semiconductor memory structure of Claim 8 wherein said wordlines are in  
2 contact with said vertical transistors by means of a conductive plug.
- 1 10. The semiconductor memory structure of Claim 8 wherein said wordlines include a  
2 conductive material, a nitride cap present atop said conductive material and nitride  
3 sidewall spacers present on exposed sidewalls of said conductive material and said  
4 nitride cap.
- 1 11. The semiconductor memory structure of Claim 8 further comprising bitline  
2 conductors formed atop said wordlines, said bitline conductors and said wordlines are  
3 isolated from each other.
- 1 12. A method for forming a semiconductor memory structure comprising the steps of:  
2

- 3 (a) forming at least one adjacent pair of trench storage memory cells present in a Si-  
4 containing substrate, each memory cell including a vertical transistor overlaying a trench  
5 capacitor and strap outdiffusions present on each vertical sidewall of the trench storage  
6 memory cells, wherein said strap outdiffusions interconnect said vertical transistor and  
7 said trench capacitor of each memory cell to said Si-containing substrate; and  
8  
9 (b) forming a punchthrough stop doping pocket between each adjacent pair of trench  
10 storage memory cells, said punchthrough stop doping pocket is centered between said  
11 strap outdiffusions and self-aligned to said trench capacitors.

1 13. The method of Claim 12 wherein step (a) includes the steps of: forming oxide filled  
2 troughs atop said Si-containing substrate; forming a patterned photoresist atop said oxide  
3 filled troughs, said patterned photoresist having openings that expose portions of an  
4 alternating pair of oxide filled troughs, while protecting the oxide filled <sup>(f)</sup>tough next to  
5 said alternating pair; removing oxide from said portions of alternating pair of oxide filled  
6 troughs so as to expose a surface of said Si-containing substrate; and etching storage  
7 trenches into exposed surfaces of said Si-containing substrate.

1 14. The method of Claim 13 further comprising forming a buried plate diffusion region  
2 about said storage trenches; lining a portion of said trenches with a node dielectric; and  
3 filling a portion of said trenches with N+ polysilicon.

1 15. The method of Claim 14 further comprising removing a portion of said N+  
2 polysilicon from said trenches to form a region of recessed N+ polysilicon; forming a  
3 strap outdiffusion region about a portion of said storage trenches; forming a top trench  
4 oxide on said recessed N+ polysilicon; forming a gate dielectric on each exposed  
5 sidewall of said storage trenches; and filling said trenches with additional N+ polysilicon  
6 thereby forming polysilicon lines.

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1 16. The method of Claim 15 further comprising forming active area resist stripes  
2 orthogonal to said trench storage memory cells and forming isolation trench regions in  
3 regions not protected by said active area resist stripes.

1 17. The method of Claim 12 wherein step (b) includes an implant process which is  
2 performed in an opening adjacent to said pair of trench storage memory cells.

1 18. The method of Claim 17 wherein said opening includes sidewall spacers.

1 19. The method of Claim 12 further comprising forming wordlines above said trench  
2 memory cells after step (b) is performed.

1 20. The method of Claim 19 further comprising forming bitline conductors above said  
2 wordlines.